16ch PHADC (C008)

- 16ch are condensed to the CAMAC width.
- As for the input signal, even which of plus and minus is to be acceptable, and moreover specify input impedance at the time of the 50Ω～5kΩ delivery, too.
- 16ch can be measured at the same time.
- Peak Hold part becomes a mini-card, and maintenance is easy for it.
- ADC is a comparative type one after another as to high-speed 12bit.
- It has analog Sum output.
- It has Discri inside, and NIM is output in HOLD-OUT. (When this output is made GATE, a self-trigger is possible as PHA.)

The voltage of the peak of the analog signal is digitized with 12bitADC. It copes with a high-speed signal because it copes with it more than gate width 500nSec, too.

< CAMAC Function >

- F(0)・A(0～15)・S1 : Data lead 0～15ch
- F(0)・A(0～15)・S1 : Data lead 0～15ch
- F(2)・A(15)・S2 : Peak Hold resetting
- F(8) : Test LAM
- F(9)・S2 : Peak Hold resetting
- F(10)・S2 : LAM Clearance
- C・S2 : Peak Hold resetting
- Z・S2 : Peak Hold resetting

![Gate input](image1)
![Input of an analog](image2)
![Mini-card output](image3)
Gate input : NIM level minimum width 500nSec  
Residual quantity pedestal : Standard 50 counts

Input of an analog : 0~2.5V (or 0~−2.5V)  
Change time : 100μSec following ~100nSec It is started.

SUM output : The addition output of 16ch input

~200nSec It is lowered 3% and under of the errors
~200nSec It is started.

Hold output : Discriminator output of the SUM

~300nSec It is lowered 3% and under of the errors

Output (NIM level)

ADC : One after another, a comparative 12bit

(about one channel 5μ sec)

Input impedance : 50Ω change is possible.

Straight line : 1LSB following

Input of resetting : NIM level minimum width 50nSec

Reset time : 800nSec

Form : CAMAC standard 1 width module

Power supply : +6V, +24V, −6V, −24V

Approve it because specifications and so on that it is refused are sometimes changed.