ＣＡＭＡＣ

１６ｃｈ　ＰＨＡＤＣ

（C008）

◎　16ch are condensed to the CAMAC width.

◎　As for the input signal, even which of plus and minus is to be acceptable, and moreover specify input impedance at the time of the 50Ω～5kΩ　delivery, too.

◎　16ch can be measured at the same time.

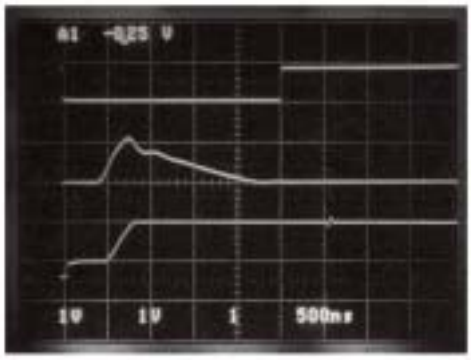
◎　Peak Hold part becomes a mini-card, and maintenance is easy for it.

◎　ADC is a comparative type one after another as to high-speed 12bit.

◎　It has analog Sum output.

◎　It has Discri inside, and NIM is output in HOLD-OUT.（When this output is made GATE, a self-trigger is possible as PHA.）

The voltage of the peak of the analog signal is digitized with 12bitADC.
It copes with a high-speed signal because it copes with it more than gate width 500nSec, too.



Gate input

Input of an analog

Mini-card output

＜　ＣＡＭＡＣ　Ｆｕｎｃｕｉｏｎ　＞

Ｆ（0）・Ａ（0～１５）・Ｓ１	:	Data lead　0～１５ｃｈ
Ｆ（0）・Ａ（0～１５）・Ｓ１	:	Data lead　0～１５ｃｈ
Ｆ（2）・Ａ（１５）・Ｓ２	:	Peak Hold resetting
Ｆ（8）	:	Test LAM
Ｆ（9）・Ｓ２	:	Peak Hold resetting
Ｆ（１０）・Ｓ２	:	LAM Clearance
Ｃ・Ｓ２	:	Peak Hold resetting
Ｚ・Ｓ２	:	Peak Hold resetting

＜ Ｓｐｅｃｉｆｉｃａｔｉｏｎｓ ＞

Gate input : NIM level minimum width 500nSec

Input of an analog : ０～２．５Ｖ（or０～－２．５Ｖ）

～１００ｎＳｅｃIt is started.

～２００ｎＳｅｃIt is lowered 3% and under of the errors

～２００ｎＳｅｃIt is started.

～３００ｎＳｅｃ It is lowered 3% and under of the errors

Input impedance : 50Ω change is possible.

Input of resetting : NIM level minimum width 50nSec

Reset time : ８００ｎＳｅｃ

Residual quantity pedestal : Standard 50 counts

Change time : １００μＳｅｃ following

SUM output : The addition output of 16ch input

Hold output : Discriminator output of the SUM output（ＮＩＭ level）

ＡＤＣ : One after another, a comparative 12bit (about one channel 5μsec)

Straight line : １ＬＳＢ following

Form : CAMAC standard 1 width module

Power supply : ＋６Ｖ、＋２４Ｖ、－６Ｖ、－２４Ｖ

Approve it because specifications and so on that it is refused are sometimes changed.